Claims

What is claimed is:

1. A method used to form a semiconductor device comprising:

forming a layer to be etched over a semiconductor wafer substrate assembly;

forming a boron-doped amorphous carbon (a-C:B) antireflective coating (ARC) layer over said layer to be etched;

patterning said a-C:B ARC layer to expose said layer to be etched;

etching said layer to be etched to pattern said layer; then

exposing said a-C:B ARC layer to an oxygen plasma.

2. The method of claim 1 further comprising heating said a-C:B ARC layer to a temperature of between about 200°C and about 380°C during said exposure of said ARC layer to said oxygen plasma.

3. The method of claim 2 further comprising exposing said ARC layer to said oxygen plasma for a duration of between about 20 seconds and about 120 seconds.

4. The method of claim 1 further comprising:

prior to patterning said a-C:B ARC layer, forming a patterned photoresist layer over said a-C:B ARC layer;

patterning said a-C:B ARC layer using said patterned photoresist layer as a pattern during said patterning of said a-C:B arc layer to expose said layer to be etched; and

exposing both said photoresist layer and said a-C:B ARC layer to said oxygen plasma.

5. The method of claim 1 further comprising introducing a fluorine-containing gas into said oxygen plasma during said exposure of said a-C:B ARC layer to said oxygen plasma.

6. The method of claim 1 wherein said layer to be etched is a dielectric layer and said method further comprises:

forming an opening in said dielectric layer during said etching of said layer to be etched; and

subsequent to exposing said a-C:B ARC layer to said oxygen plasma, forming a conductive layer within said opening in said dielectric layer.

7. The method of claim 1 wherein said exposure of said a-C:B ARC layer to said oxygen plasma forms an ashed a-C:B layer and said method further comprises exposing said ashed a-C:B layer to a solution comprising both phosphoric acid and ammonium fluoride.

8. A method for patterning a layer to be etched which overlies a semiconductor wafer, comprising:

forming a boron-doped amorphous carbon layer on said layer to be etched;

forming a photoresist layer on said boron-doped amorphous carbon layer;

patterning said photoresist layer and said boron-doped amorphous carbon layer; and

etching said layer to be etched to pattern said layer to be etched using said pattern of said patterned boron-doped amorphous carbon layer as a pattern.

9. The method of claim 8 further comprising removing said photoresist layer and said boron-doped amorphous carbon layer by:

exposing said photoresist layer and said boron-doped amorphous carbon layer to an oxygen plasma to form an ashed photoresist layer and an ashed boron-doped amorphous carbon layer subsequent to etching said layer to be etched; and

exposing said ashed photoresist layer and said ashed boron-doped amorphous carbon layer to an acid.

10. The method of claim 9 further comprising introducing a fluorine-containing gas into said oxygen plasma during said exposure of said boron-doped amorphous carbon layer to said oxygen plasma.

11. The method of claim 9 further comprising exposing said ashed photoresist layer and said ashed boron-doped amorphous carbon layer to a solution comprising phosphoric acid and ammonium fluoride during said exposure of said ashed photoresist layer and ashed said boron-doped amorphous carbon layer to said acid.

12. An in-process semiconductor device, comprising:

an antireflective layer comprising amorphous carbon having a boron concentration of between about 0.1 atom % and about 20 atom %.

13. The in-process semiconductor device of claim 12 further comprising said antireflective layer comprising amorphous carbon having a boron concentration of between about 0.1 atom % and about 10 atom %.

14. The in-process semiconductor device of claim 12 further comprising a photoresist layer on said antireflective layer.

15. The in-process semiconductor device of claim 14 further comprising:

a conductive contact location; and

a dielectric layer having an opening therein,

wherein said antireflective layer and said photoresist layer each have openings therein, wherein said openings in said dielectric layer, said antireflective layer, and said photoresist layer are aligned and expose said conductive contact location.

16. The in-process semiconductor device of claim 15 wherein said conductive contact location is a conductive contact pad electrically coupled with a doped region within a semiconductor wafer.